IN THE CLAIMS

Please amend the claims to be in the form as follows:

Claim 1 (original): A decoder comprising a plurality of tuners for receiving data from different sources, each having an associated demultiplexer controlled to select a portion of a received signal corresponding to a selected channel or channels, the demultiplexers being arranged to output to a remultiplexer configured to determine selected signal portions that have overlapping addresses, to reallocate addresses of the signal portions so there is no overlap, and to multiplex the signal portions for supply to a common interface slot.

Claim 2 (original): A decoder according to claim 1, in which the common interface slot is arranged to route the multiplexed signal portions through any inserted common interface card and then on to a demultiplexer for dividing the multiplexed signal portions and routing at least a part of the divided output to its destination.

Claim 3 (original): A decoder according to claim 1, further comprising a switching unit connecting the demultiplexers to a number of remultiplexers, the switching unit being arranged to accept signal portions from the demultiplexers and to selectively switch each signal portion to one or more of the remultiplexers, each remultiplexer being configured to determine those signal portions that have overlapping addresses, to reallocate addresses of the signal portions so there is no overlap, and to multiplex the signal portions for supply to a common interface slot.

Claim 4 (original): A decoder according to claim 3, in which each remultiplexer is connected to a different common interface slot.

Claim 5 (original): A decoder according to claim 3, in which a signal portion is switched to a remultiplexer in dependence on its content.

Claim 6 (original): A decoder according to claim 3, in which a signal portion is switched

to a remultiplexer in dependence on its source.

Claim 7 (original): A decoder according to claim 1, in which an address comprises a channel identifier.

Claim 8 (original): A decoder according to claim 1, in which upon reallocating an address, a new index stream is created and embedded within the signal portion.

Claim 9 (new): A decoder according to claim 1, wherein each of the demultiplexers is connected to a switching unit that routes signals from the demultiplexers to the remultiplexer.

Claim 10 (new): A decoder according to claim 9, wherein, routing of the switching unit is performed based on a combination of network and channel identifiers. being arranged to accept signal portions from the demultiplexers and to selectively switch each signal portion to one or more of the remultiplexers, wherein the remultiplexers are configured to determine those signal portions that have overlapping addresses, to reallocate addresses of the signal portions so there is no overlap, and to multiplex the signal portions for supply to the common interface slot.

Claim 11 (new): A decoder comprising

a plurality of tuners that are each operatively coupled to receive data from a plurality of different sources,

a plurality of demultiplexers associated with the plurality of tuners, the demultiplexers being controlled to select a portion of a received signal from the sources,

a remultiplexer configured to receive an output of the demultiplexers, determine if the portions have overlapping addresses, and to reallocate addresses of the portions so there is no overlap, and to multiplex the portions.

Claim 12 (new): A decoder according to claim 11, in which the multiplexed the portions are supplied to a common interface slot that is arranged to route the multiplexed signal portions through any inserted common interface card and also to a demultiplexer for dividing the multiplexed signal portions.

Claim 13 (new): A decoder according to claim 11, comprising a switching unit connecting the demultiplexers to a number of remultiplexers, the switching unit being arranged to accept signal portions from the demultiplexers and to selectively switch each signal portion to one or more of the remultiplexers, each remultiplexer being configured to determine those signal portions that have overlapping addresses, to reallocate addresses of the signal portions so there is no overlap, and to multiplex the signal portions for supply to a common interface slot.

Claim 14 (new): A decoder according to claim 13, in which each remultiplexer is connected to a different common interface slot.

Claim 15 (new): A decoder according to claim 13, in which a signal portion is switched to a remultiplexer in dependence on its content.

Claim 16 (new): A decoder according to claim 13, in which a signal portion is switched to a remultiplexer in dependence on its source.

Claim 17 (new): A decoder according to claim 11, in which an address comprises a channel identifier.

Claim 18 (new): A decoder according to claim 11, in which upon reallocating an address, a new index stream is created and embedded within the signal portion.

Claim 19 (new): A decoder according to claim 11, wherein each of the demultiplexers is connected to a switching unit that routes signals from the demultiplexers to the remultiplexer.

Claim 20 (new): A decoder according to claim 19, wherein, routing of the switching unit is performed based on a combination of network and channel identifiers. being arranged to accept signal portions from the demultiplexers and to selectively switch each signal portion to one or more of the remultiplexers, wherein the remultiplexers are configured to determine those signal portions that have overlapping addresses, to reallocate addresses of the signal portions so there is no overlap, and to multiplex the signal portions for supply to the common interface slot.